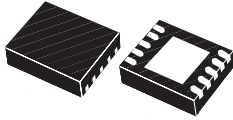


## Electronic load switch for power line



DFN10L (3x3 mm)

[Maturity status link](#)[STELPD01](#)

### Features

- Wide input voltage range: 4 V to 18 V
- 17.5 V typical output overvoltage clamp
- Absolute maximum voltage of 23.5 V
- 5 A maximum continuous current
- Adjustable current limit with circuit breaker functionality
- Thermal protection
- Input undervoltage lockout
- Low inrush current during startup
- Integrated 40 mΩ Power FET
- EN/Fault pin
- Adjustable slew rate for output voltage
- Gate control pin for reverse current blocking FET
- Latch or auto-retry
- Available in DFN10L (3x3 mm) package

### Applications

- Hot-Swap, Hot-Plug protection
- Industrial Systems
- VBUS management for Type-C and USB PD applications

### Description

The **STELPD01** is an integrated electronic power switch for power rail protection applications.

It is able to precisely detect and react to overcurrent and overvoltage conditions.

When an overload condition occurs, the device goes into an open state, disconnecting the load from the power supply. An external power MOSFET can be driven to manage the power loss protection in case of fault condition.

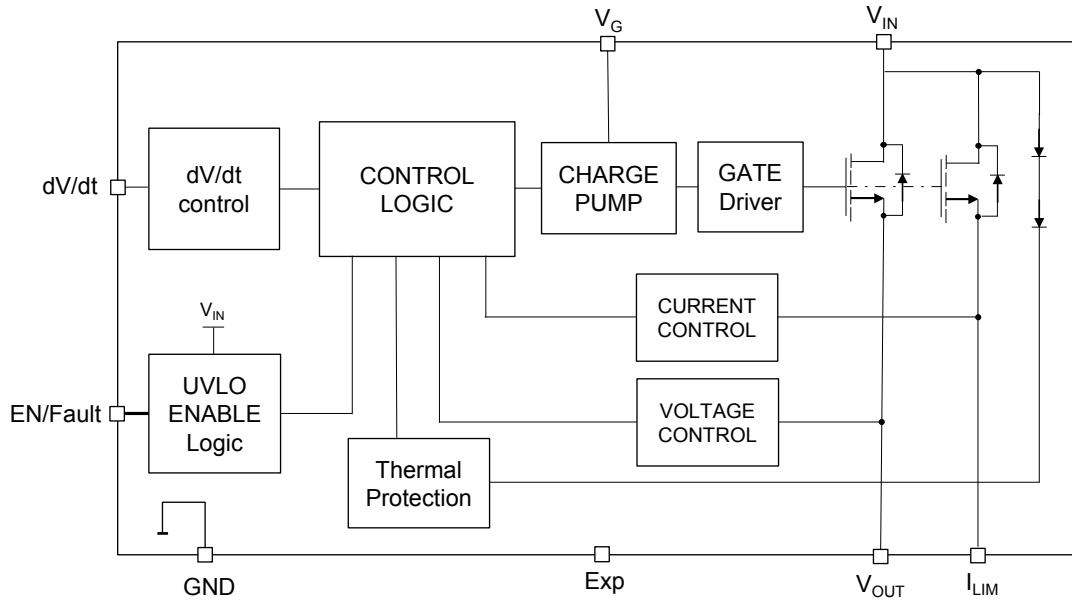
In case of overvoltage on the input, the device regulates the output to a preset 17.5 V value.

Undervoltage lockout prevents the load from malfunction, keeping the device off if the rail voltage is too low.

The **STELPD01** features an adjustable turn-on slew-rate, which is useful to keep the in-rush current under control during startup and hot-swap operations.

# 1 Diagram

Figure 1. Block diagram



## 2 Pin configuration

Figure 2. Pin connection (top view)

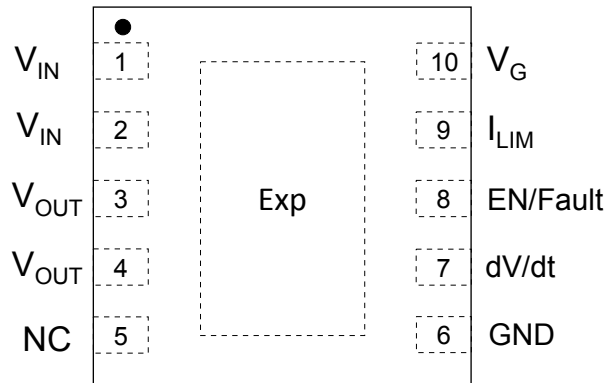
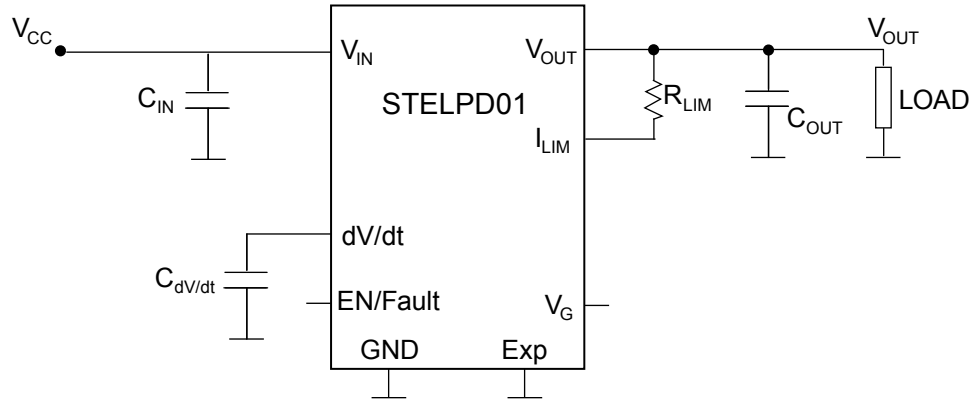
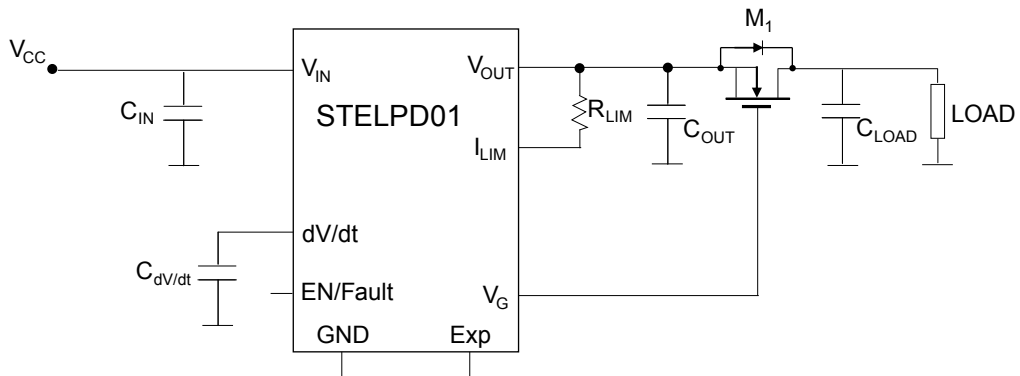


Table 1. Pin description

| Pin n° | Symbol          | Function  |
|--------|-----------------|---|
| 1-2    | $V_{IN}$        | Positive input voltage.   |
| 3-4    | $V_{OUT}$       | Connected to the source of the internal power MOSFET.   |
| 5      | NC              | Not connected.  |
| 6      | GND             | Ground.   |
| 7      | dV/dt           | Soft-start adjustment pin. The internal dV/dt circuit controls the slew rate of the output voltage at turn-on. The internal capacitor allows a fixed ramp-up time but an external capacitor can be added to this pin to increase the ramp time. If an additional capacitor is not required, this pin should be left open.   |
| 8      | EN/Fault        | The EN/Fault pin is a tri-state, bi-directional interface.<br>During normal operation the pin can be left floating, it is internally pulled up to 5 V. It can be used to disable the output of the device by pulling it to ground using an open drain or open collector device.<br>See <a href="#">Section 6.1</a> , <a href="#">Section 6.5</a> , <a href="#">Section 6.6</a> and <a href="#">Section 6.7</a> for other specific functions of this pin according to the device versions. |
| 9      | $I_{LIM}^{(1)}$ | An $R_{LIM}$ resistor between this pin and the $V_{OUT}$ pin sets the overload current limit threshold.   |
| 10     | $V_G$           | External gate driver pin. An external power MOSFET can be connected to implement the reverse current protection.  |
|        | Exp             | The device's package uses the center pad as a thermal conduit. This pad should be connected to an adequate spread of copper. GND connection is suggested.   |

1. Important: missing or shorted  $R_{LIM}$  causes current limit circuit malfunction and may lead to device damage.

### 3 Application circuits

**Figure 3. Typical application circuit**

**Figure 4. Typical application circuit with reverse current protection**

**Table 2. Typical application components**

| Symbol      | Value       | Description                 | Note   |
|-------------|-------------|-----------------------------|--|
| $C_{IN}$    | 1 $\mu$ F   | Input capacitor             | This value should be increased depending on input inductance and load current. |
| $C_{dV/dt}$ | 560 pF      | Soft-start capacitor        | This value depends on the desired soft-start time.                             |
| $R_{LIM}$   | 51 $\Omega$ | Current limitation resistor | This value depends on the desired current limit threshold.                     |
| $C_{OUT}$   | 10 $\mu$ F  | Output capacitor            |  |

## 4 Maximum ratings

**Table 3. Absolute maximum ratings**

| Symbol             | Parameter   | Value                         | Unit |
|--------------------|---|-------------------------------|------|
| V <sub>IN</sub>    | Power supply input voltage                          | -0.3 to 23.5                  | V    |
| V <sub>OUT</sub>   | Output voltage                                      | -0.3 to V <sub>IN</sub> + 0.3 | V    |
| I <sub>LIM</sub>   | Current limit resistor pin voltage                  | -0.3 to 23.5                  | V    |
| EN/Fault           | EN/Fault pin voltage                                | -0.3 to 7                     | V    |
| dV/dt              | dV/dt pin voltage                                   | -0.3 to 7                     | V    |
| V <sub>G</sub>     | External gate driver pin voltage                    | -0.3 to 23.5                  | V    |
| T <sub>J-OP</sub>  | Operating junction temperature range <sup>(1)</sup> | -40 to 125                    | °C   |
| T <sub>J-MAX</sub> | Maximum junction temperature                        | 125                           | °C   |
| T <sub>STG</sub>   | Storage temperature range                           | -55 to 150                    | °C   |
| T <sub>LEAD</sub>  | Lead temperature (soldering) 10 sec                 | 260                           | °C   |

1. The thermal limit is set above the maximum thermal rating. It is not recommended to operate the device at temperatures greater than the maximum ratings for extended periods.

**Note:** Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All values are referred to GND.

**Table 4. Thermal data**

| Symbol            | Parameter  | Value | Unit |
|-------------------|--|-------|------|
| R <sub>thJA</sub> | Thermal resistance junction-ambient <sup>(1)</sup> | 53    | °C/W |
| R <sub>thJC</sub> | Thermal resistance junction-case                   | 18    | °C/W |

1. Based on JESD51-7, 4-layer PCB.

**Table 5. ESD performance**

| Symbol | Parameter              | Test conditions | Value | Unit |
|--------|------------------------|-----------------|-------|------|
| ESD    | ESD protection voltage | HBM             | 2     | kV   |
|        |                        | CDM             | 500   | V    |

**Table 6. Recommended operating condition**

| Symbol           | Parameter  | Value     | Unit |
|------------------|--|-----------|------|
| V <sub>IN</sub>  | Operating power supply input voltage                             | 4 to 16.8 | V    |
| I <sub>D</sub>   | Maximum continuous current T <sub>A</sub> = 25 °C <sup>(1)</sup> | 5         | A    |
| C <sub>IN</sub>  | Minimum input capacitor  | 1         | μF   |
| C <sub>OUT</sub> | Minimum output capacitor   | 1         | μF   |

1. The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J(MAX)</sub>, the junction-to-ambient thermal resistance θ<sub>JA</sub>, and the ambient temperature T<sub>A</sub> and can be estimated by: P<sub>D(MAX)</sub> = (T<sub>J(MAX)</sub> - T<sub>A</sub>) / θ<sub>JA</sub>. Exceeding the maximum allowable power dissipation produces overheating that may cause thermal shutdown.

## 5 Electrical characteristics

$V_{IN} = 5\text{ V}$ ,  $V_{EN/Fault} = 5\text{ V}$ ,  $C_{IN} = 10\text{ }\mu\text{F}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{dV/dt} = \text{floating}$ ,  $R_{LIM} = 22\text{ }\Omega$ ;  $T_J = 25\text{ }^\circ\text{C}$ ; unless otherwise specified.

**Table 7. Electrical characteristics**

| Symbol                               | Parameter                                      | Test conditions   | Min. | Typ. | Max. | Unit          |
|--------------------------------------|--|---|------|------|------|---------------|
| <b>Under/Oversvoltage protection</b> |  |   |      |      |      |               |
| $V_{CLAMP}$                          | Clamping voltage                               | $I_{OUT} = 10\text{ mA}$  | 16.8 | 17.5 | 18.2 | V             |
| $V_{UVLO}$                           | $V_{IN}$ undervoltage lockout                  | Turn-on, $V_{IN}$ rising  | 2.85 | 2.9  | 2.95 | V             |
|                                      |  | Hysteresis  |      | 150  |      | mV            |
| <b>Power MOSFET</b>                  |  |   |      |      |      |               |
| $T_{DELAY}$                          | Delay time                                     | Enabling of chip to soft-start beginning (10% of $V_{OUT}$ ), No $C_{dV/dt}$          |      | 165  |      | $\mu\text{s}$ |
| $R_{DSon}$                           | On-resistance <sup>(1)</sup>                   | $T_J = 25\text{ }^\circ\text{C}$ , $I_{OUT} = 500\text{ mA}$                          |      | 42   | 52   | m $\Omega$    |
|                                      |  | $T_J = 85\text{ }^\circ\text{C}$ <sup>(2)</sup>                                       |      | 50   |      |               |
|                                      |  | $V_{IN} = 15\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$ , $I_{OUT} = 500\text{ mA}$ |      | 40   | 50   |               |
|                                      |  | $V_{IN} = 15\text{ V}$ , $T_J = 85\text{ }^\circ\text{C}$ <sup>(2)</sup>              |      | 48   |      |               |
| $V_{OFF}$                            | Off-state output voltage                       | $V_{IN} = 18\text{ V}$ , $R_L = \text{infinite}$ , EN/Fault connected to ground       |      | 1    | 3    | mV            |
| <b>Current limit</b>                 |  |   |      |      |      |               |
| $I_{LIM}$                            | Overcurrent limit threshold                    | $R_{LIM} = 22\text{ }\Omega$  |      | 5.15 |      | A             |
|                                      |  | $R_{LIM} = 51\text{ }\Omega$  |      | 3    |      |               |
| <b>dV/dt circuit</b>                 |  |   |      |      |      |               |
| dV/dt                                | Output voltage ramp time                       | From 10% to 90% of $V_{OUT}$ , No CdV/dt  |      | 500  |      | $\mu\text{s}$ |
| <b>Blocking FET gate driver</b>      |  |   |      |      |      |               |
| $I_{FET}$                            | External FET charging current                  | Device on   |      | 30   |      | $\mu\text{A}$ |
| $V_{FETmax}$                         | External FET clamp voltage                     | $V_{IN} = 9\text{ V}$ , $V_G - V_{OUT}$   |      | 4.6  |      | V             |
| $R_{FETdisch}$                       | External FET discharging current               | $V_{EN/Fault} = 0\text{ V}$ , $V_G = V_{IN}$  |      | 7.5  |      | mA            |
| $T_{PLP}$                            | PLP intervention time                          | From EN/Fault = 0 V or $V_{IN} < V_{UVLO}$ to $V_G < 1\text{ V}$                      |      | 1    |      | $\mu\text{s}$ |
| <b>EN/Fault</b>                      |  |   |      |      |      |               |
| $V_{IL}$                             | Low level input voltage threshold              | Output disabled   |      |      | 0.4  | V             |
| $V_{I(INT)}$                         | Intermediate level input voltage               | Thermal fault, output disabled  | 750  | 825  | 900  | mV            |
| $V_{IH}$                             | High level input voltage threshold             |   | 2.55 |      |      | V             |
| $V_{I(MAX)}$                         | High state maximum voltage                     | $V_{IN} = 5\text{ V}$   |      | 4.9  |      | V             |
|                                      |  | $V_{IN} = 15\text{ V}$  |      | 4.95 |      |               |
| $I_{IL}$                             | Low level input current (sink)                 | $V_{EN/Fault} = 0\text{ V}$   |      | -100 | -140 | $\mu\text{A}$ |
| $I_{IH}$                             | High level leakage current for external switch | $V_{EN/Fault} = 5\text{ V}$   |      | 1    |      | $\mu\text{A}$ |

| Symbol                     | Parameter                        | Test conditions                                   | Min. | Typ. | Max. | Unit |
|----------------------------|----------------------------------|---|------|------|------|------|
| <b>Thermal protection</b>  |                                  |   |      |      |      |      |
| $T_{SHDN}$                 | Thermal shutdown <sup>(3)</sup>  |   |      | 165  |      | °C   |
| $T_{SHDN\_HYS}$            | Hysteresis                       |   |      | 20   |      | °C   |
| <b>Current consumption</b> |                                  |   |      |      |      |      |
| $I_{BIAS}$                 | Bias current, device operational | $V_{IN} = 5\text{ V}$                             |      | 300  |      | μA   |
|                            |                                  | $V_{IN} = 15\text{ V}$                            |      | 350  |      |      |
|                            | Bias current, fault mode         | $V_{IN} = 5\text{ V}$                             |      | 115  |      | μA   |
|                            |                                  | $V_{IN} = 15\text{ V}$                            |      | 135  |      |      |
|                            | Bias current, off mode           | $V_{IN} = 5\text{ V}, V_{EN/Fault} = 0\text{ V}$  |      | 200  |      | μA   |
|                            |                                  | $V_{IN} = 15\text{ V}, V_{EN/Fault} = 0\text{ V}$ |      | 225  |      |      |

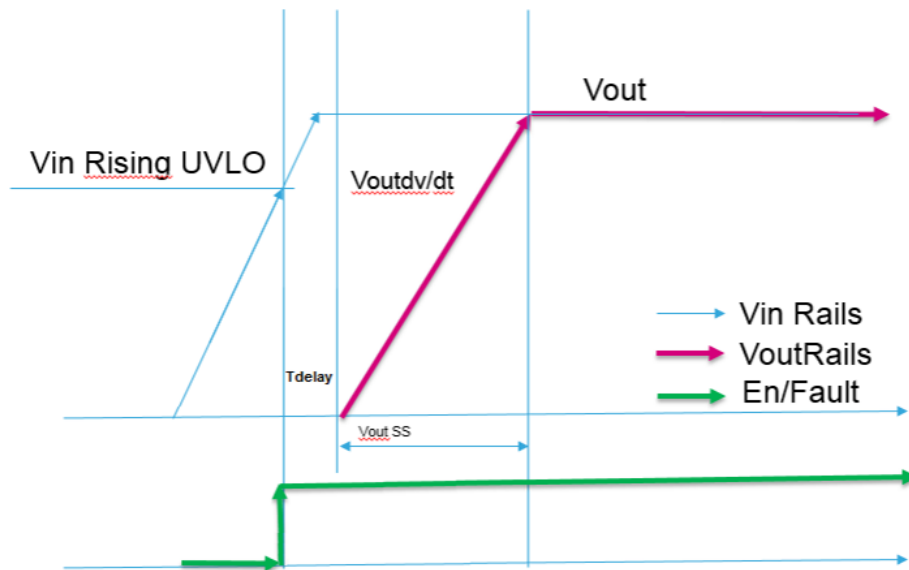
1. Pulsed test.
2. Values across temperature range are guaranteed by design/correlation and tested in production only at ambient temperature.
3. Guaranteed by design, but not tested in production.

## 6 Functional description

### 6.1 Turn-on and soft start-up feature

When the input voltage is applied and it reaches  $V_{UVLO}$  (undervoltage lockout threshold) value, the EN/Fault pin goes up to the high state (if left floating) and the internal control circuitry is enabled to perform the output start-up ramp. See the figure below.

Figure 5. Typical startup sequence for STELPD01 and STELPD01A

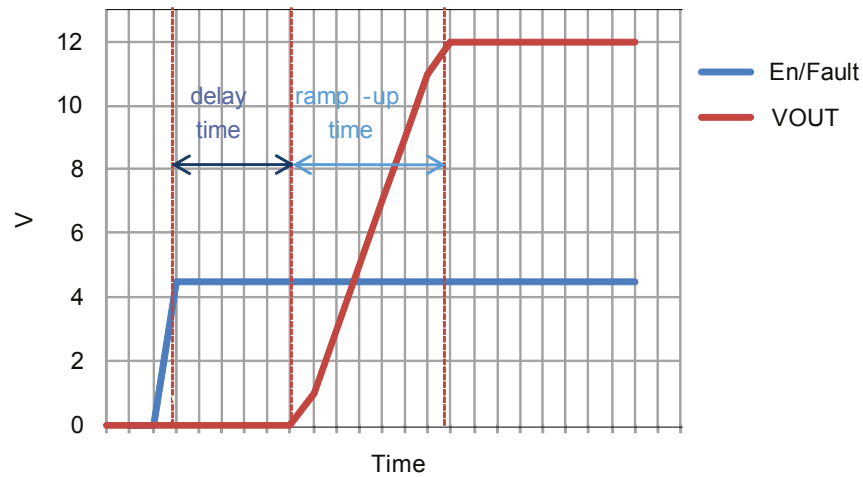


The start-up procedure starts with an initial delay time of typically **165  $\mu$ s**, then the output voltage is supplied with a slope defined by the internal  $dV/dt$  circuitry. If no additional capacitor is connected to  $dV/dt$  pin, the ramp-up time ( $V_{OUT}$  from 10% to 90%) is around **500  $\mu$ s** with  $V_{IN} = 5$  V.

The inrush current profile can be controlled through a dedicated soft-start circuit. Connecting a capacitor between the  $C_{dV/dt}$  pin and GND allows the modification of the output voltage ramp-up time. Given the desired time interval  $\Delta t$  during which the output voltage goes from 10% to 90% of  $V_{OUT}$ , the capacitance to be added on the  $C_{dV/dt}$  pin can be calculated using the following theoretical formula.

$$\Delta t[ms] = 0.0024 \times V_{IN}[V] \times C_{dV/dt}[pF] + 0.1 \times V_{IN}[V] \quad (1)$$



**Figure 6. Delay time and V<sub>OUT</sub> ramp-up time**

**Table 8. Rise time vs. C<sub>dv/dt</sub>, V<sub>IN</sub> = 5 V**

| C <sub>dv/dt</sub> [pF] | 0   | 22   | 33   | 47   | 100 | 180  | 270  | 470  | 1000 |
|-------------------------|-----|------|------|------|-----|------|------|------|------|
| Rise time [ms]          | 0.5 | 0.76 | 0.89 | 1.06 | 1.7 | 2.66 | 3.74 | 6.14 | 12.5 |

*Note:* Above table shows typical rise times obtained with available capacitor values. Values with C<sub>dv/dt</sub> ≠ 0 are guaranteed by design/correlation and not tested in production.

## 6.2 Maximum load at startup

Depending on supply voltage, load and output capacitance, it is possible that during startup the power dissipation reaches the maximum power protection and the output is shut down before the startup is completed. Increasing soft-start time, the inrush current is reduced and overtemperature fault is avoided.

Adjustable soft-start time is very useful in those applications where a single power supply serves several loads connected to the same rail with a big equivalent capacitive load. Therefore, it is important to determine the right start-up time and in-rush current to limit the dynamic power stresses and avoid thermal shutdown during startup.

## 6.3 Normal operating condition

The STELPD01 behaves like a power switch, buffering the circuitry on its output with the same voltage shown at its input, except for a small voltage fall due to the N-channel MOSFET R<sub>DSon</sub>.

## 6.4 Output voltage clamp

This internal protection circuit clamps the output voltage to a maximum safe value, typically 17.5 V, if the input voltage exceeds the V<sub>CLAMP</sub> threshold. In this condition, the device regulates the output voltage, therefore power dissipation increases and according to load current, the thermal shutdown can occur.

## 6.5 Current limiting

During operation, if the load current reaches the I<sub>LIM</sub> overload threshold, an overload is detected.

The current limiting circuit opens the power MOSFET disconnecting the load.

Typical reaction time of overcurrent control loop is 1.5 μs. This time considers the delay between the instant when output current reaches I<sub>LIM</sub> threshold and the activation of current control loop that acts on the gate of integrated FET to open the power path.

On the latched versions (STELPD01), the EN/Fault pin of the device is automatically set to the intermediate voltage V<sub>I(NT)</sub>, during V<sub>out</sub> falling edge, in order to signal the overload event to the system controller.

The device can be reset from this condition either by cycling the supply voltage or by pulling down the EN pin below the V<sub>IL</sub> threshold and then releasing it.

On the auto-retry version (STELPD01A), the EN/Fault pin is pulled down and the device attempts to turn on output channel with soft-start ramp after a delay time of 100  $\mu$ s.

The  $R_{LIM}$  value for achieving the requested current limitation can be estimated by using the following table together with the graph in [Figure 9](#) and [Figure 10](#).

**Table 9.  $I_{LIM}$  vs.  $R_{LIM}$**

|                        |      |      |     |      |    |     |     |      |     |
|------------------------|------|------|-----|------|----|-----|-----|------|-----|
| $R_{LIM}$ [ $\Omega$ ] | 15   | 22   | 36  | 39   | 51 | 75  | 120 | 220  | 300 |
| $I_{LIM}$ [A]          | 6.45 | 5.15 | 3.9 | 3.55 | 3  | 2.4 | 2.1 | 1.55 | 1.4 |

*Note:* Missing or shorted  $R_{LIM}$  causes current limit circuit malfunction and may lead to device damage.

*Note:*  $R_{LIM}$  value higher than 300  $\Omega$  can be used but as shown in [Figure 9](#) the  $I_{LIM}$  vs.  $R_{LIM}$  relationships is flat.

## 6.6 Thermal shutdown function

If the device temperature exceeds the thermal shutdown threshold ( $T_{SHDN}$ ), typically 165  $^{\circ}$ C, the power MOSFET is turned off and the load is disconnected.

On the latched version (STELPD01), the EN/Fault pin of the device is automatically set to the intermediate voltage  $V_{I(INT)}$ , in order to signal the overtemperature event to the system controller.

The device can be reset from this condition either by cycling the supply voltage or by pulling down the EN pin below the  $V_{IL}$  threshold and then releasing it.

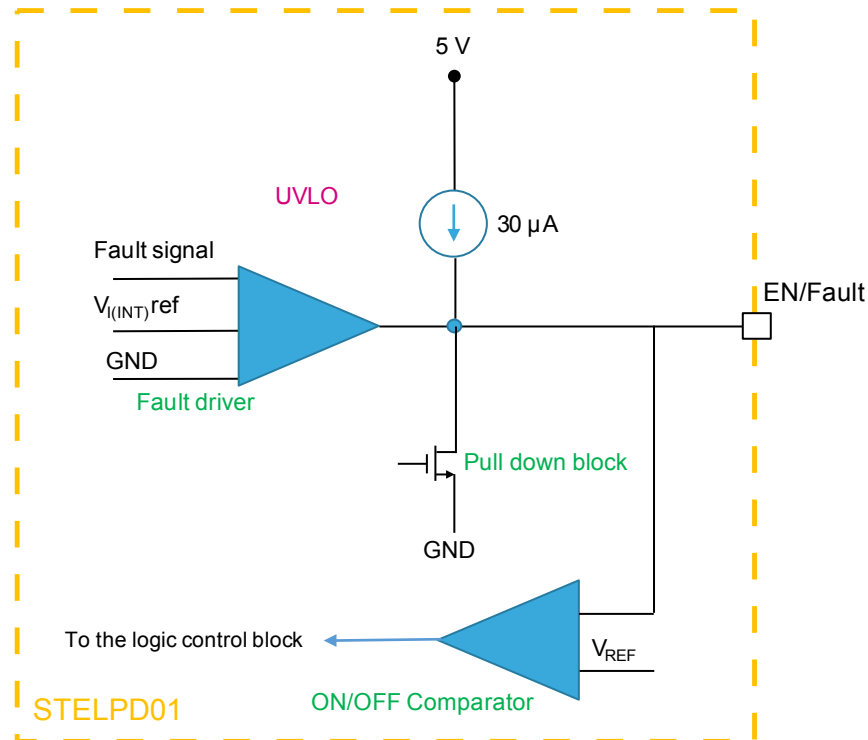
On the auto-retry version (STELPD01A), the EN/Fault pin is set low, and the auto-retry circuit attempts to restart the device with soft-start ramp once the die temperature is reduced to 145  $^{\circ}$ C typ. (165  $^{\circ}$ C minus the hysteresis value, 20  $^{\circ}$ C typ.).

## 6.7 EN/Fault pin

The EN/Fault pin has the dual function of controlling the output of the device and providing information about the device status to the application.

When it is used as a standard Enable pin, it can be connected to an external open-drain or open-collector device. In this case, when it is pulled at low logic level, the device turns the output off, when it is left floating the device turns on the output, since it has internal pull-up circuitry.

In case of a fault, on the latched versions, this pin is set to the intermediate voltage  $V_{I(INT)}$ , this signal can be provided to a monitor circuit, informing it that a fault event has occurred or it can be directly connected to the EN/Fault pins of other devices of the same family on the same application in order to achieve a simultaneous enable/disable feature. In case of UVLO event ( $V_{IN} = V_{UVLO} - V_{hyst}$ ) an internal pull-down block is activated in order to keep the device in off-state.

**Figure 7. EN/Fault driver circuit**


## 6.8 External gate driver function for reverse blocking

The STELPD01 provides a dedicated gate drive signal on the VG pin which can be used to control an external blocking MOSFET for reverse-current protection (RCP). See [Figure 4](#).

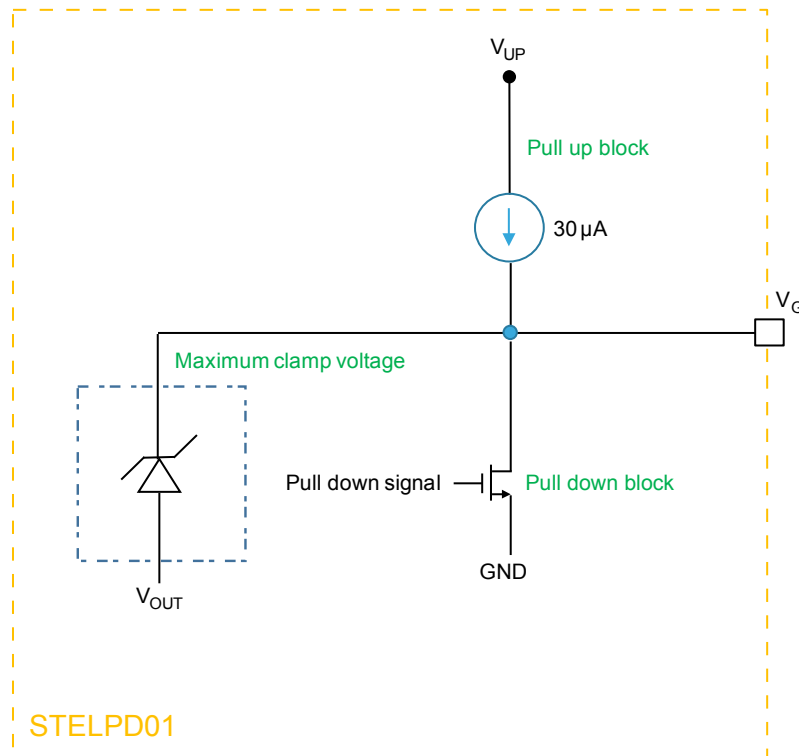
When the internal control circuitry is enabled to perform output start-up ramp, the  $V_{gate}$  pin is pulled up by External FET charging current  $I_{FET}$  to the charge pump voltage referred to the  $V_{in}$  voltage in order to guarantee the activation of external FET.

If the input voltage reaches  $V_{clamp}$  threshold the  $V_{gate}$  voltage is also clamped to a safe value of  $V_{out} + 5.5$  V. See [Figure 23](#).

Reverse current protection is activated in case  $V_{IN}$  falls below the undervoltage lockout (UVLO), the enable (EN) voltage falls below the low-level threshold, or a fault event occurs.

For example, as  $V_{CC}$  drops during input power removal, the device turn off internal FET and it sinks current from the gate of the external FET to quickly turn it off, therefore blocking any current flow from the load to the input side.

Figure 8. External gate driver circuit



## 6.9 External capacitors and application guidelines

Input and output capacitors are mandatory to guarantee device control loop stability and reduce the transient effects of stray inductances which may be present on the input and output power paths. In fact, when the STELPD01 interrupts the current flow, input inductance generates a positive voltage spike on the input, and output inductance generates a negative voltage spike on the output. To reduce the effects of such transients, a  $C_{IN}$  capacitor of at least  $1 \mu\text{F}$  must be connected between the input pin and GND, and located as close as possible to the device.

For the same reason, a  $C_{OUT}$  capacitor of at least  $1 \mu\text{F}$  must be connected at the output port.

When the device is powered by a power line made up of very long wires, where input inductance is higher than  $1 \mu\text{H}$ , the input capacitor should be increased.

It is recommended to provide for additional protections and methods for addressing these transients, such as:

- Minimizing inductance of the input and output tracks
- TVS diodes on the input to absorb inductive spikes
- Schottky diode on the output to absorb negative spikes
- Combination of ceramic and electrolytic capacitors on the input and output

## 7 Typical characteristics

$V_{IN} = 5\text{ V}$ ,  $V_{EN/Fault} = \text{floating}$ ,  $R_{LIM} = 51\ \Omega$ ,  $C_{IN} = 2.2\ \mu\text{F}$ ,  $C_{OUT} = 10\ \mu\text{F}$ ,  $C_{dV/dt} = 560\ \text{pF}$ ,  $T_A = 25\ ^\circ\text{C}$ , unless otherwise specified.

Figure 9.  $I_{LIM}$  vs.  $R_{LIM}$

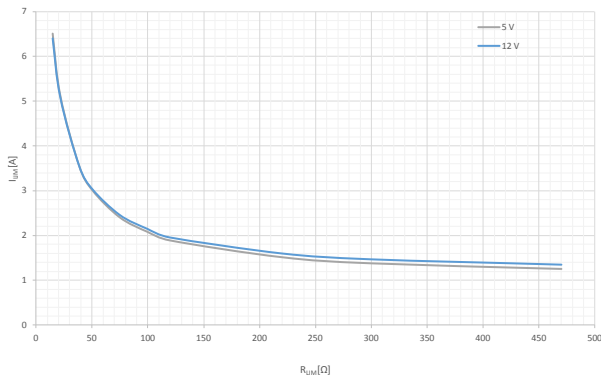


Figure 10.  $I_{LIM}$  vs.  $R_{LIM}$  (magnification)

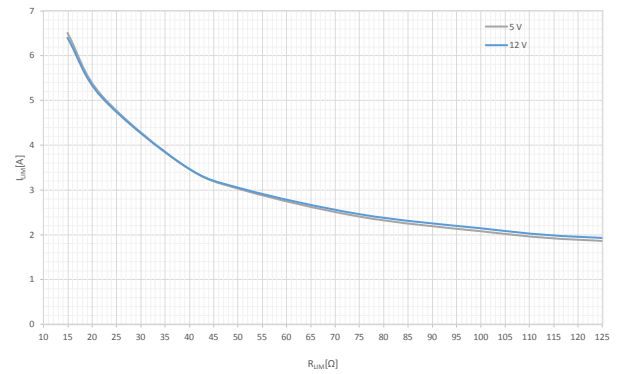


Figure 11. Bias current vs. temperature (ON Mode)

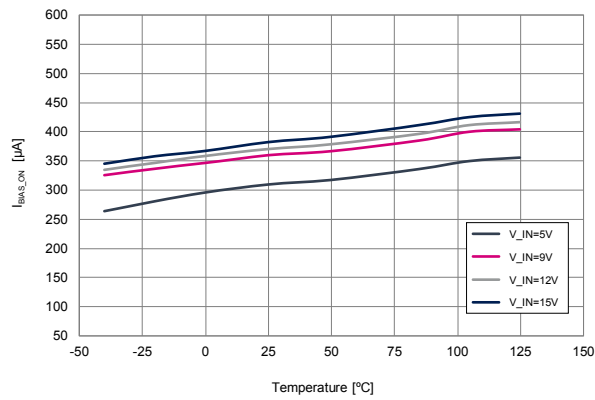
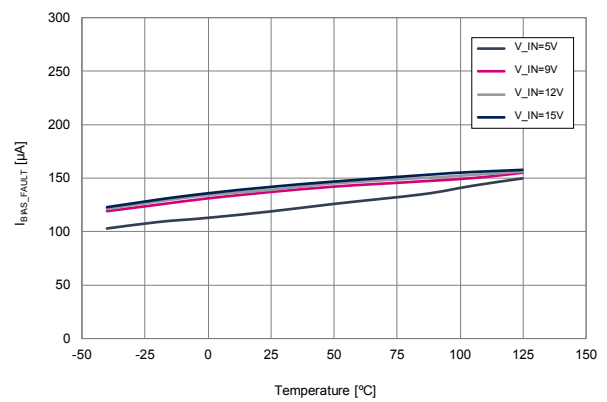
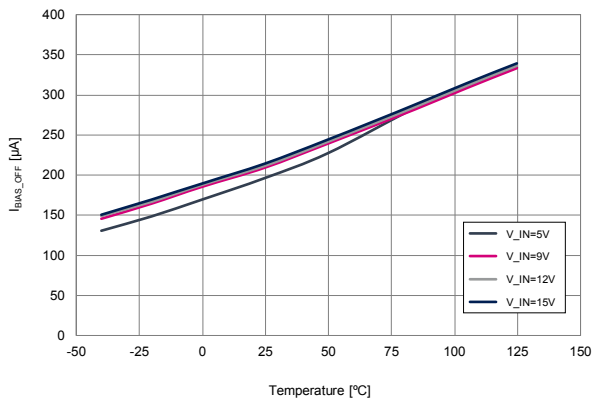


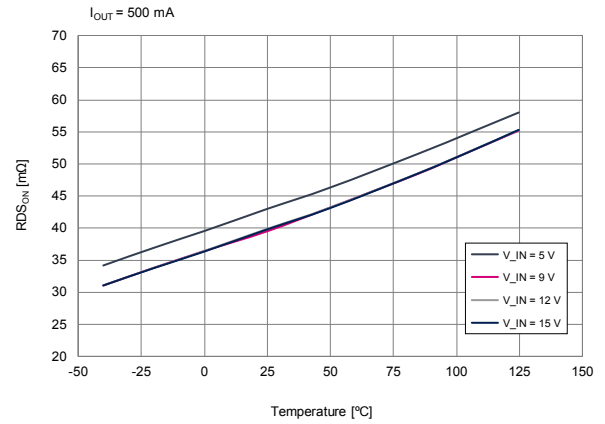
Figure 12. Bias current vs. temperature (Fault Mode)



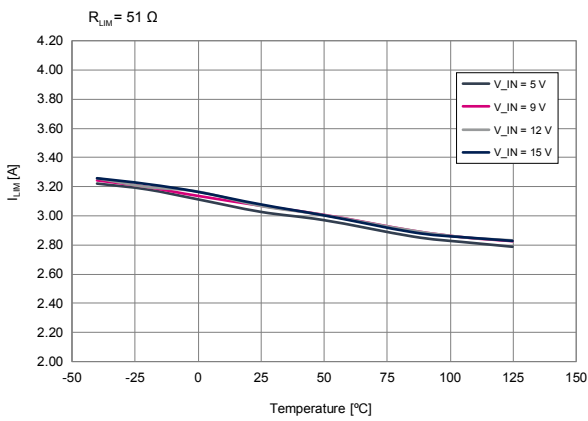
**Figure 13. Bias current vs. temperature (OFF Mode)**



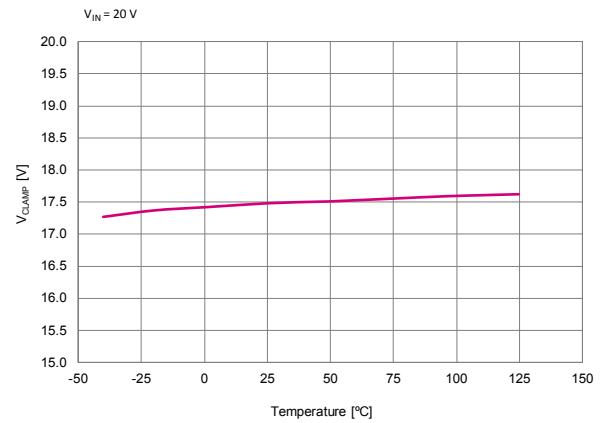
**Figure 14. R\_DS\_ON vs. temperature**



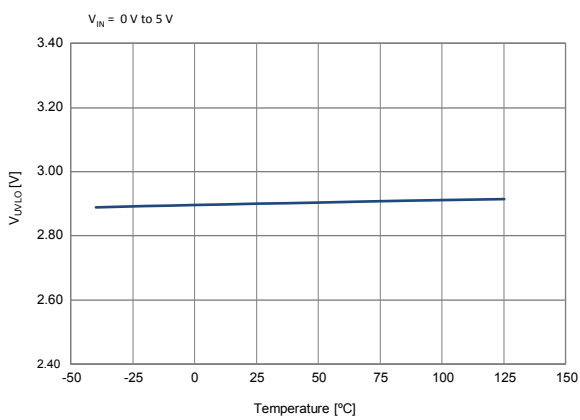
**Figure 15. I\_LIM vs. temperature**



**Figure 16. Clamping voltage vs. temperature**



**Figure 17. UVLO vs. temperature**



**Figure 18. UVLO Hysteresis vs. temperature**

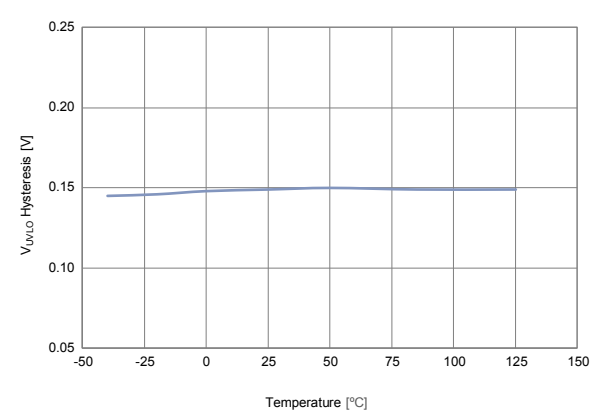


Figure 19. EN/Fault pin thresholds vs. temperature

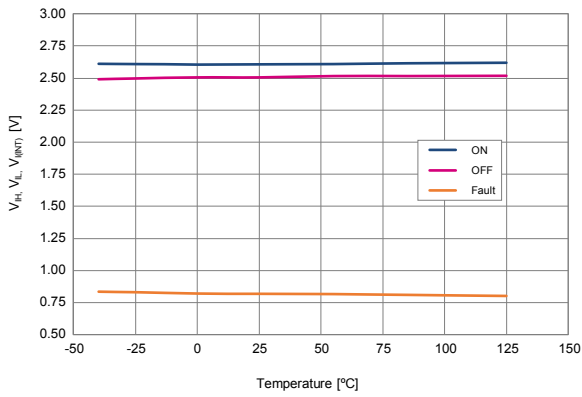


Figure 20. EN/Fault pull-up voltage vs. temperature

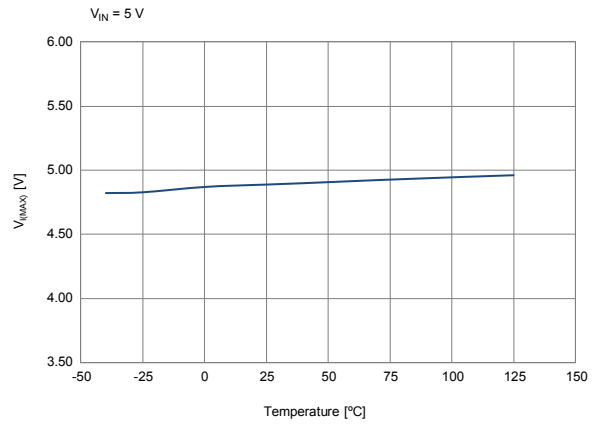


Figure 21. EN/Fault pin current vs. temperature (EN/Fault to GND)

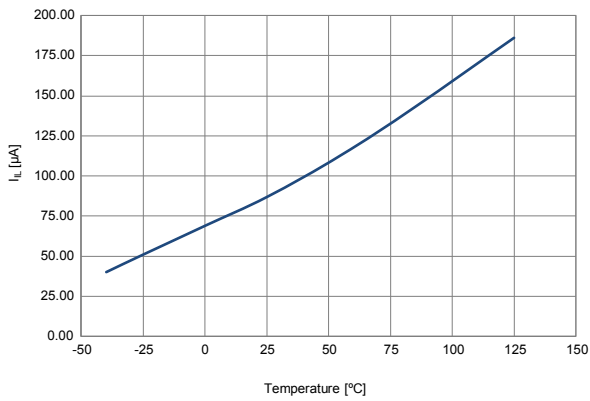


Figure 22. Soft-start time vs. temperature (no Cdv/dt)

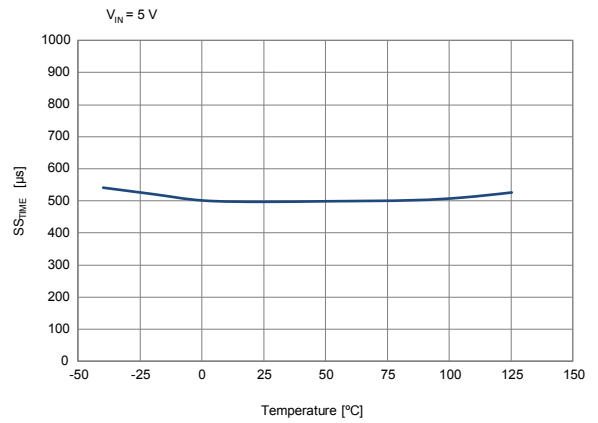


Figure 23. External FET clamp voltage (V<sub>FETmax</sub>) vs. input voltage

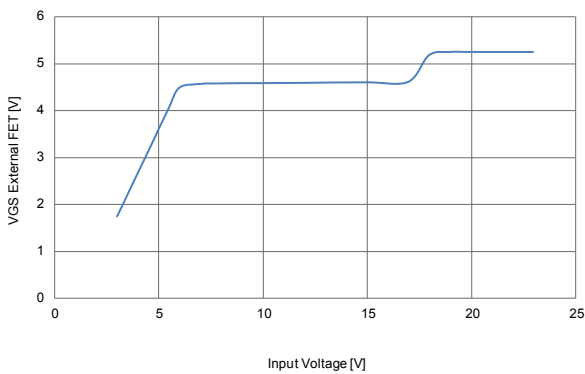


Figure 24. Startup with no load

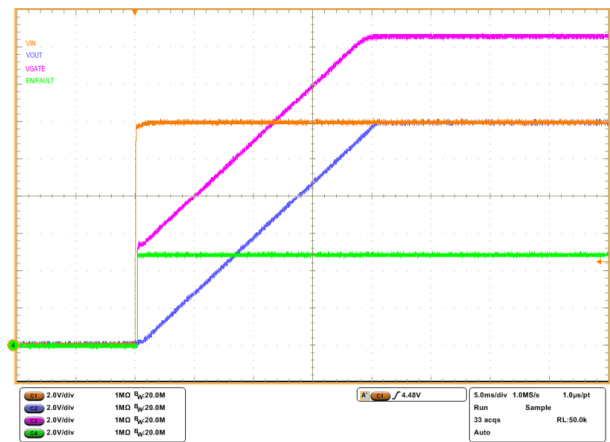
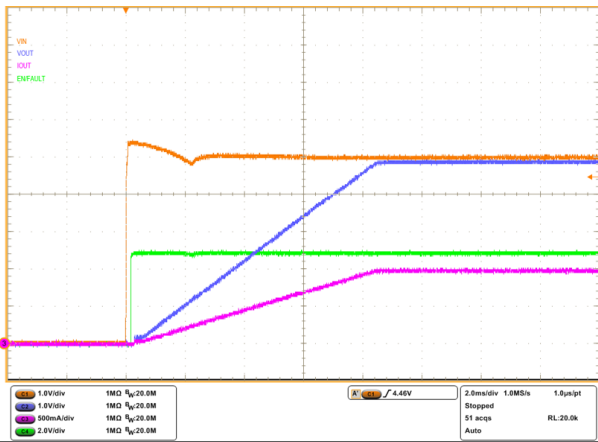
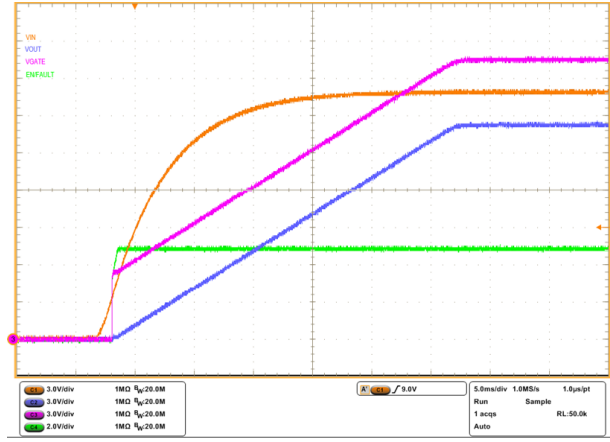


Figure 25. Startup with  $R_{LOAD} = 5 \Omega$



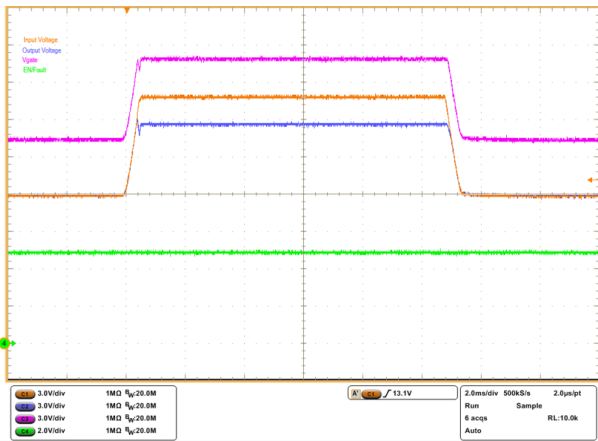
$V_{IN}$  = from 0 V to 5 V (Hot-plug connection)

Figure 26. Startup into voltage clamp



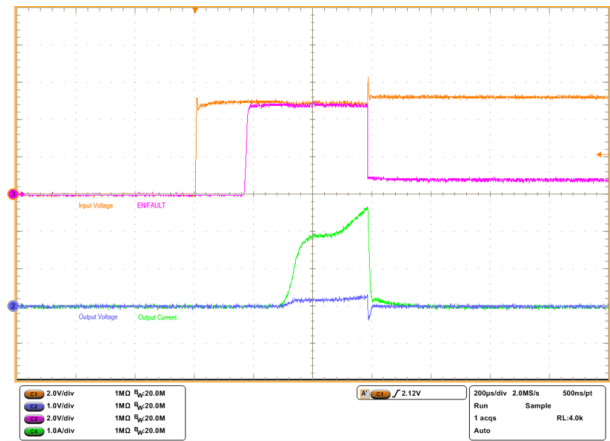
$V_{IN}$  = from 0 V to 20 V,  $I_{OUT} = 0$  mA

Figure 27. Voltage clamp during operation



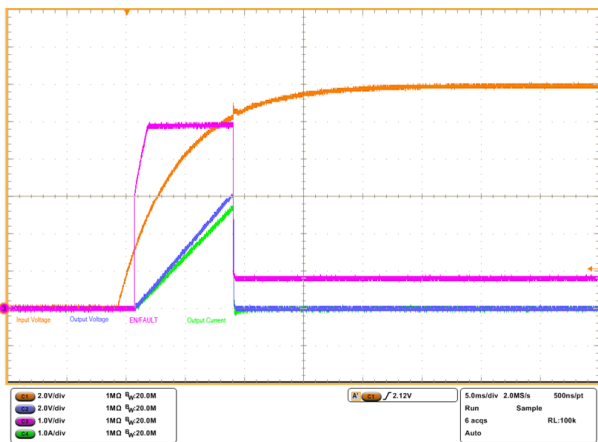
$V_{IN}$  = from 12 V to 20 V,  $I_{OUT} = 100$  mA

Figure 28. Start-up into output short-circuit



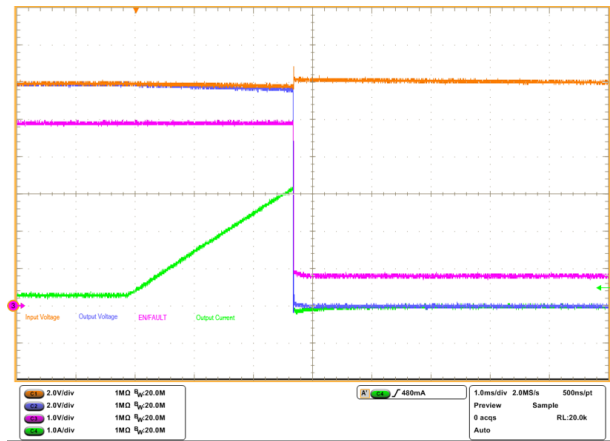
$V_{IN}$  = from 0 V to 5 V,  $V_{OUT}$  = shorted to GND,  $R_{LIM} = 100 \Omega$

Figure 29. Startup into overload



$V_{IN}$  = from 0 V to 12 V,  $R_{LOAD} = 2.2 \Omega$ ,  $R_{LIM} = 100 \Omega$

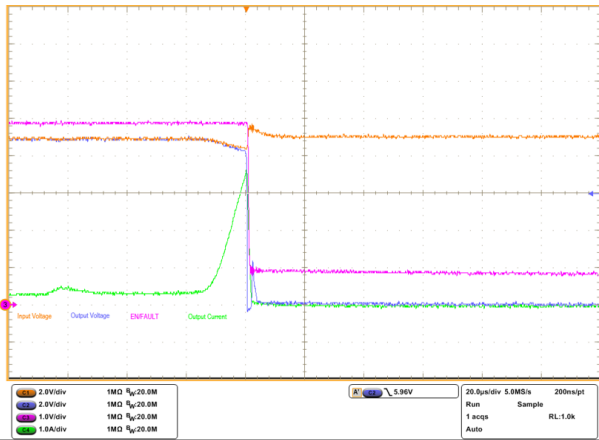
Figure 30. Overcurrent protection during operation (latched version)



$V_{IN} = 12$  V,  $I_{LOAD} =$  CC Load from 300 mA to current limit,  $R_{LIM} = 51 \Omega$

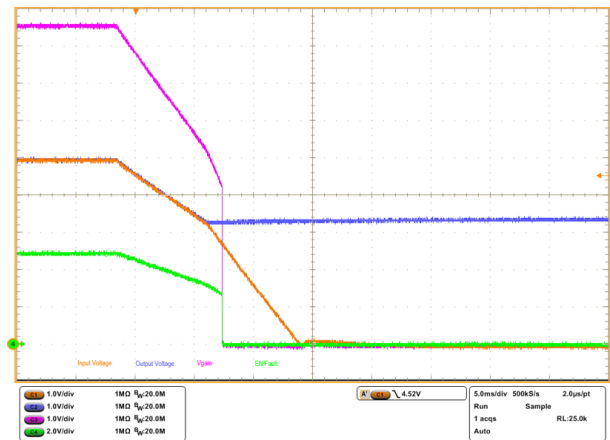


Figure 31. Output short-circuit during operation (latched version)



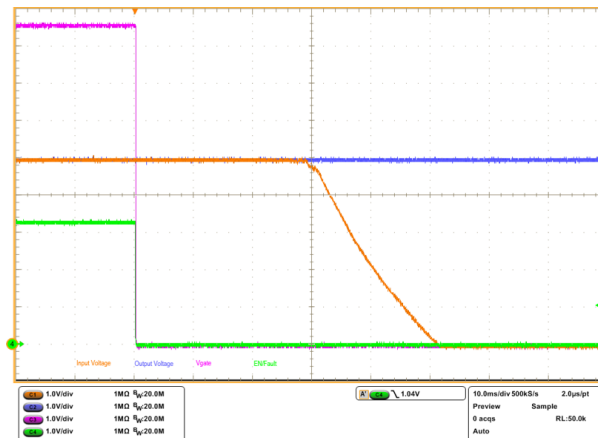
$V_{IN} = 9\text{ V}$ ,  $I_{LOAD} = \text{CC Load from } 300\text{ mA to short circuit}$ ,  $R_{LIM} = 51\ \Omega$

Figure 32. Power loss protection through UVLO



$V_{IN} = \text{from } 5\text{ V to floating}$ ,  $I_{OUT} = 0\text{ mA}$ ,  $C_{OUT} = 100\ \mu\text{F}$

Figure 33. Power loss protection through EN/Fault



$V_{IN} = \text{from } 5\text{ V to } 0\text{ V}$ ,  $V_{EN/Fault} = \text{from } 3.3\text{ V to GND}$ ,  $I_{OUT} = 0\text{ mA}$ ,  $C_{OUT} = 100\ \mu\text{F}$

## 8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

### 8.1 DFN10L (3x3 mm) package information

**Figure 34. DFN10L (3x3 mm) package outline**

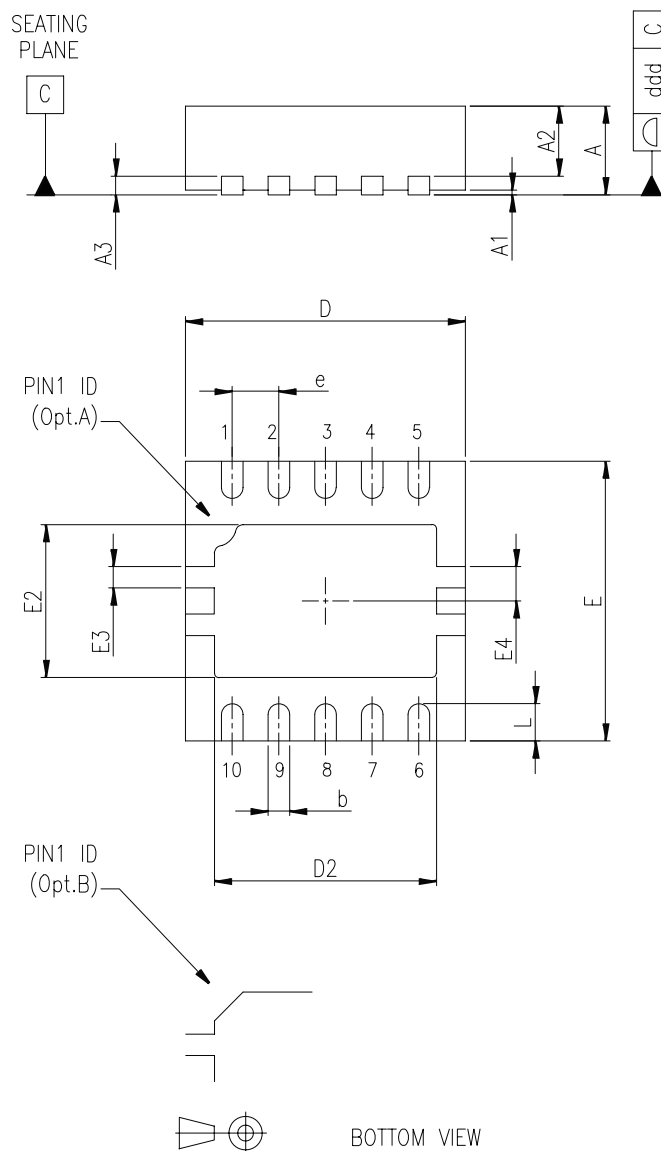
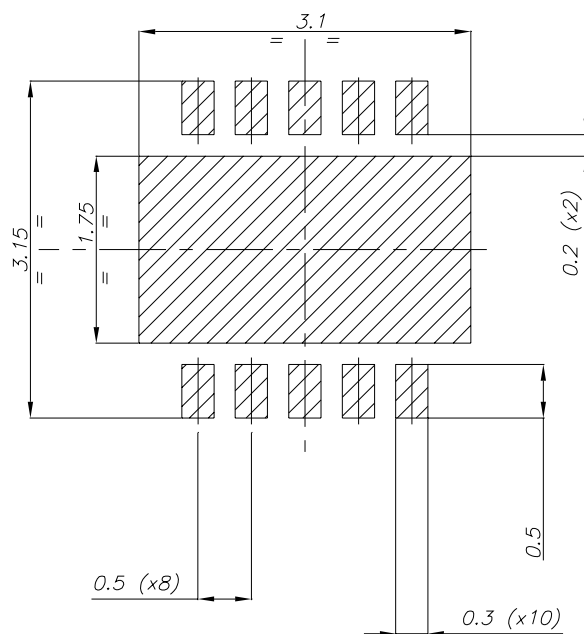


Table 10. DFN10L (3x3 mm) mechanical data

| Dim. | mm    |      |      |
|------|-------|------|------|
|      | Min.  | Typ. | Max. |
| A    | 0.80  | 0.90 | 1.00 |
| A1   |       | 0.02 | 0.05 |
| A2   | 0.55  | 0.65 | 0.80 |
| A3   |       | 0.20 |      |
| b    | 0.18  | 0.25 | 0.30 |
| D    | 2.85  | 3.00 | 3.15 |
| D2   | 2.20  |      | 2.70 |
| E    | 2.85  | 3.00 | 3.15 |
| E2   | 1.40  |      | 1.75 |
| E3   | 0.230 |      |      |
| E4   | 0.365 |      |      |
| e    |       | 0.50 |      |
| L    | 0.30  | 0.40 | 0.50 |
| ddd  |       |      | 0.08 |

Figure 35. DFN10L (3x3 mm) recommended footprint



## 8.2 DFN10 (3 x 3 mm) packing information

Figure 36. DFN10 (3 x 3 mm) reel drawing outline

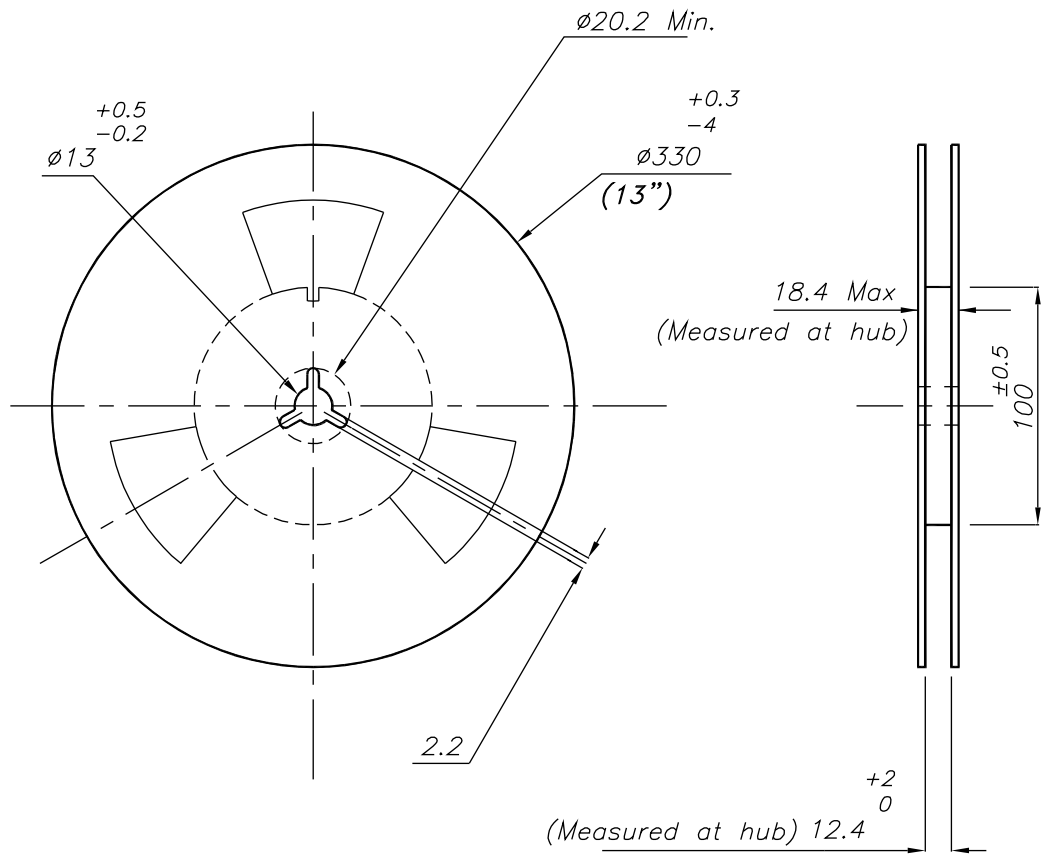


Figure 37. DFN10 (3 x 3 mm) carrier tape

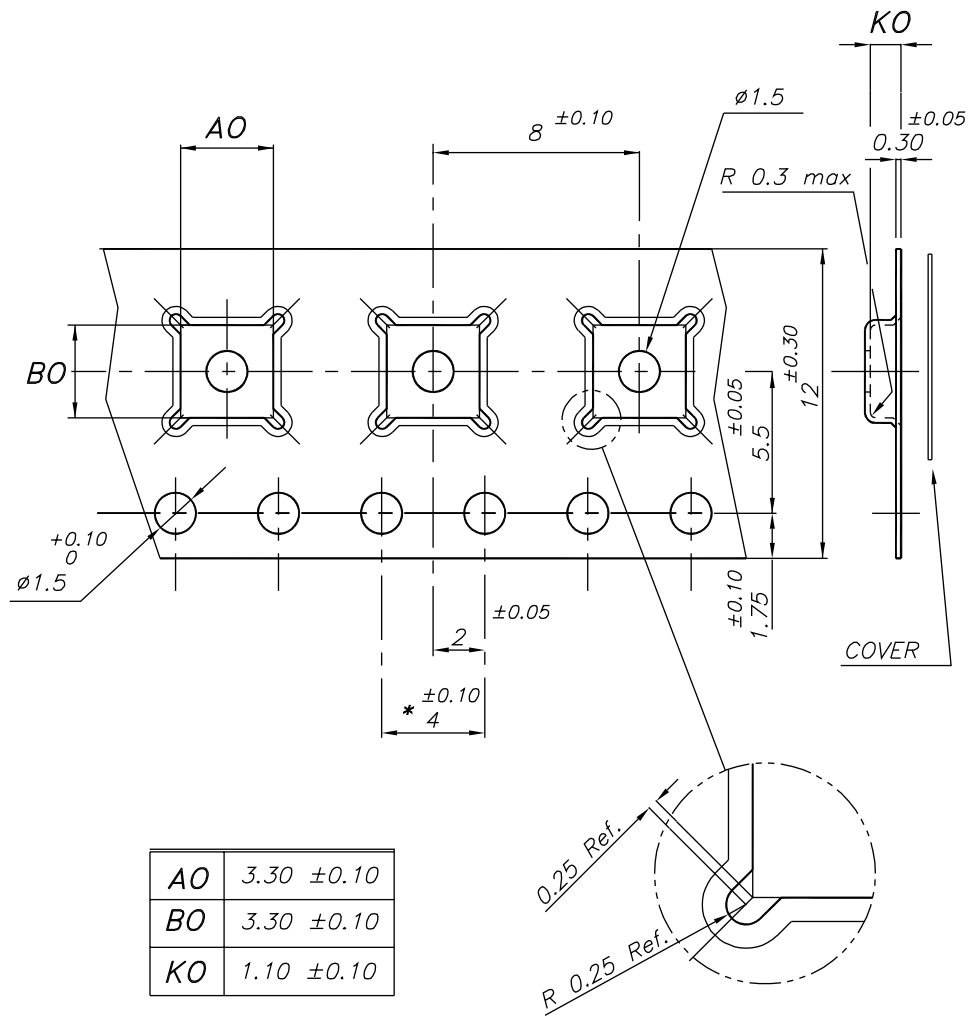
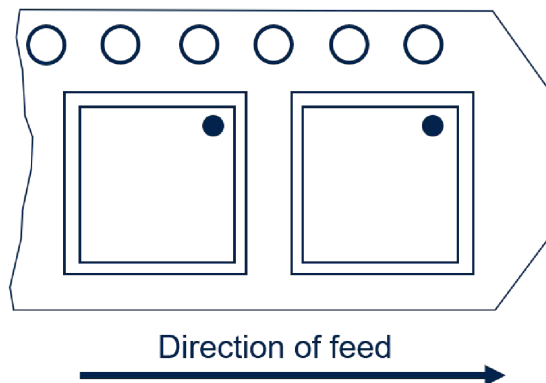


Figure 38. DFN10 (3 x 3 mm) device orientation in tape



## 9 Ordering information

**Table 11. Order codes**

| Order code                  | Package         | Packaging     | Marking | Response to thermal and overcurrent fault | EN/Fault at startup      |
|-----------------------------|-----------------|---------------|---------|---|--------------------------|
| STELPD01PUR                 | DFN10L-(3x3 mm) | Tape and reel | EPD1    | Latch-off                                 | High (Automatic startup) |
| STELPD01APUR <sup>(1)</sup> |                 |               | TBD     | Auto-retry                                |                          |

1. Version under development. Contact ST sales offices.

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## Revision history

**Table 12. Document revision history**

| Date        | Revision | Changes          |
|-------------|----------|------------------|
| 17-Jan-2022 | 1        | Initial release. |

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